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(54) External storage apparatus having a circuit for selecting a communication protocol

(57) The present invention enables connection and a high-speed access to a plurality of electronic apparatuses having different types of built-in interfaces.

The present invention provides an external storage apparatus including: storage means 22; an interface controller A21 and an interface controller B24, each having a different type of built-in interface control block for

carrying out a data writing and/or reading into/from the storage means 22; and connection means 26 for selecting and connecting one of the interface controller A21 and the interface controller B24 to the electronic apparatus. It is preferable that the connection means 26 be constructed so as to select one of the interface controller A21 and the interface controller B24 according to a control from the electronic apparatus.

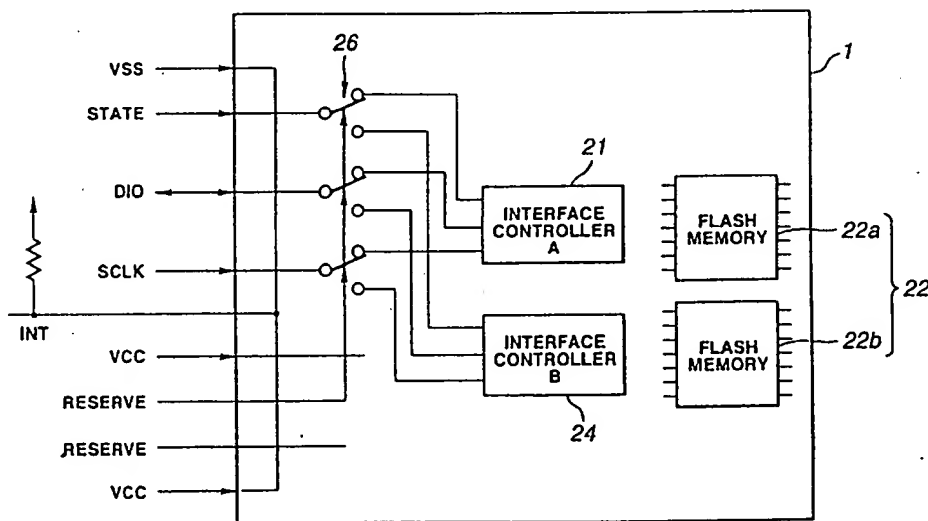


FIG.3

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Description

The present invention relates to external storage apparatus, for example apparatus for storing data from an electronic device.

Conventionally, when an electronic apparatus such as a computer, for example, is used as a main storage device, an external storage apparatus is used as an additional capacity to this main storage apparatus. As this external storage apparatus, there can be exemplified a magnetic tape, a magnetic disc, magneto-optical disc, paper tape, card type memory, and the like. Among them, the card type memory is especially widely used because of its comparatively high transfer rate.

The card type memory has a built-in storage means and interface control block for writing and reading a data to/from the storage means. By connecting the interface control block to an interface in the electronic apparatus serving as the main storage device, the card type memory functions as an external storage apparatus of the electronic apparatus.

However, if the interface in the electronic apparatus and the interface control block in the card type memory have different interface types which can be controlled, the electronic apparatus cannot carry out direct writing and/or reading of a data into/from the card type memory.

To cope with this, as shown in Fig. 1, it is necessary to employ a conversion adapter 54 for connection between an electronic apparatus (not depicted) and a card type memory 53 including an interface controller C51 having a built-in predetermined interface control block and storage means 52 consisting of a plurality of memories such as flash memory 52a, 52b, or the like.

The conversion adapter 54 contains an interface controller D56 having a built-in interface control block capable of controlling the interface in the electronic apparatus; and a built-in serial interface 57, for example, for matching the aforementioned interface control block with the interface control block in the card type memory 53.

However, when the conversion adapter 54 is used, a conversion processing is required by the interface before reaching the flash memories 52a, 52b in the card type memory 53 from the electronic apparatus, which increases the access time.

This invention provides an external storage apparatus for storing a data from an electronic apparatus, comprising: storage means; interface control blocks of a plurality of types for carrying out a data writing and/or reading into/from said storage means; and connection means for selecting and connecting one of said plurality of interface control blocks to said electronic apparatus.

Further respective aspects and features of the invention are defined in the appended claims.

Embodiments of the present invention can provide an external storage apparatus which enables a high-speed access and can be connected without the use of a conversion adapter to a plurality of electronic appara-

tuses having different types of built-in interface.

An external storage apparatus according to embodiments of the present invention serves for storing a data from an electronic apparatus and includes: storage means; interface control blocks of a plurality of types for carrying out a data writing and/or reading into/from the storage means; and connection means for selecting and connecting one of the plurality of interface control blocks to the electronic apparatus.

Note that in the external storage apparatus, it is preferable that the aforementioned connection means be controlled from the electronics apparatus, so as to select one of the interface control blocks of plurality of types.

In the external storage apparatus, for storing a data from an electronic apparatus, there are preferably provided storage means; interface control blocks of a plurality of types for carrying out a data writing and/or reading into/from the storage means; and connection means for selecting and connecting one of the plurality of interface control blocks to the electronic apparatus. Consequently, it is possible to connect the external storage apparatus to a plurality of electronic apparatuses having different types of built-in interfaces, without using an adapter.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Fig. 1 is a block diagram showing a conventional card type memory and an adapter.

Fig. 2 is a perspective view showing a card type memory according to the present invention.

Fig. 3 is a block diagram showing a configuration of the card type memory according to the present invention.

Fig. 4 is a block diagram showing an enlarged configuration of an interface controller of the card type memory according to the present invention.

Hereinafter, explanation will be given on the present invention applied to a card type memory.

That is, the card type memory according to the present invention serves for storing a data from an electronic apparatus (not depicted) such as a computer, a still image pickup apparatus, acoustic apparatus, and a video apparatus. As shown in Fig. 2, the card type memory 1 according to the present embodiment is formed from a synthetic resin into a thin card shape having a rectangular plane.

Furthermore, in the card type memory 1 according to the present embodiment uses an interface for controlling a serial interface, thus reducing a number of external terminals 2, which in turn reduces the size of the card type memory 1 itself, so as to define a rectangular plane having a shorter side length which is half or less than half of a longer side length. For example, the shorter side is 21.5 mm and the longer side is 50 mm.

The card type memory 1 has a plurality of indenta-

tions 3 formed at one end of the longer side direction, so as to open in one main surface 1a of the two opposing main surfaces, and external terminals 2 are formed so as to be exposed at the bottoms of the indentations 3.

It should be noted that in this card type memory 1, as has been described above, an interface control block is used for controlling a serial interface, and accordingly, 9 external terminals 2 are provided. To cope with this, three indentations 3 are formed, so that three of the external terminals 2 are formed at the bottom of each indentations 3.

That is, this card type memory 1 is inserted into an electronic apparatus in the longer side direction, so that the aforementioned external terminals 2 are electrically connected to the electronic apparatus.

Moreover, the card type memory 1 has an erroneous erase preventing member 4 at the opposite end not having the external terminals 2. This erroneous erase preventive member 4 is engaged with an erroneous erase preventing switch (not depicted) which is contained inside the card type memory 1 and will be detailed later. This erroneous erase preventing switch is turned ON and OFF when it is slidably moved in the shorter side direction which intersects at a right angle to the insertion direction of the card type memory 1.

Furthermore, the card type memory 1 has a lock cut-off portion 5 formed at one side 1b parallel to the longer side direction, i.e., the insertion direction of the card type memory 1. The lock cut-off portion 5 is engaged with a convex formed on the electronic apparatus (not depicted) for locking so as to prevent removal of the card type memory 1 from the electronic apparatus.

Furthermore, a cut-off portion 6 is formed in the end side of the card type memory 1 having the external terminals, so as to define a slanting plane to the longer side of the insertion direction of the card type memory 1, thus preventing erroneous insertion of the card type memory 1.

As shown in Fig. 3, the card type memory 1 according to the present embodiment includes an interface controller A21, an interface controller B24, and storage means 22 which are all built in the card type memory 1. The storage means 22 consists of a plurality of memories such as flash memories 22a and 22b, for example, which belongs to a type of ROM (read only memory) into which a data can also be written. The interface controller A21 and the interface controller B24 are respectively connected to the flash memories 22a and 22b.

In the card type memory 1, the interface controller A21 has a built-in predetermined interface control block for controlling a predetermined serial interface, and the interface controller B24 has a built-in interface control block for controlling a serial interface of a different type from that of the aforementioned interface control block, such as USB (Universal Serial Bus) or IEEE 1394.

Furthermore, in the card type memory 1, there is provided connection means 26 for selecting one of the interface controller A21 and the interface controller B24,

so as to be connected to the aforementioned electronic apparatus (not depicted).

It should be noted that the connection means 26 is controlled by the electronic apparatus (not depicted) to select the interface controller.

More specifically, the following procedure is carried out. That is, the card type memory 1 according to the present embodiment, as has been described above, uses the serial interface control block for controlling a serial interface and according, has 9 signal lines including a State (status signal) line, DIO (Data In Out) line, SCLK (serial clock) line, and two signal lines reserved, which respectively correspond to the external terminals. For each of the signals lines for supplying respective signals from the electronic apparatus such as State (status signal), DIO (data in out), and SCLK (serial clock), a switch is provided to select one of the interface controller A21 and the interface controller B24. The switches constitute connection means 26. One of the two reserved signal lines from the electronic apparatus is used as a control line for switching which is controlled by a control signal specifying switching to one of the interface controller A21 and the interface controller B24.

Here, in the card type memory 1, the interface controller A21 or the interface controller B24 has a configuration as follows. It should be noted that here the interface controller A21 is shown as an example in Fig. 4. Fig. 4 shows an enlarged configuration of the interface controller A21.

The interface controller A21 decides whether the erroneous erase preventing switch 43 is set to recordable or disabled mode prior to writing a signal (data) supplied from an electronic apparatus (not depicted) into the storage means 22. The data is written in the storage means 22 only if the switch is set to the recordable mode.

Here, more specifically, the interface controller A21 includes: a serial/parallel - parallel/serial interface sequencer (hereinafter, referred to as an S/P & P/S sequencer) 31; a page buffer 32; a flash interface sequencer (hereinafter, referred to as a flash I/F sequencer) 33; an ECC encoder/decoder 34 for carrying out an error correction processing; a command generator 35 for generating a predetermined control command; a configuration ROM (read only memory) 36; and an oscillator 37 for supplying a clock to respective circuits.

The S/P & P/S sequencer 31 is selectively connected by connection means (not depicted) via the signal lines of State (status signal), DIO (data in out), and SCLK (serial clock) to the serial interface of the electronic apparatus. Consequently, the S/P & P/S sequencer is supplied from the electronic apparatus with the State (status signal), SCLK (serial clock), and a control data.

The S/P & P/S sequencer 31 converts a serial data supplied via the DIO (data in out) signal line from the electronic apparatus, into a parallel data in synchronization with the serial clock supplied via the aforementioned SCLK (serial clock) signal line. Among the data

converted into a parallel data, the S/P & P/S sequencer 31 supplied, for example, a control data to the command generator 35 and other data to the page buffer 32.

That is, the aforementioned S/P & P/S sequencer 31 and the command generator 35 correspond to the predetermined interface control block.

The page buffer 32 is a buffer memory for storing a data supplied from the S/P & P/S sequencer 31 on page (512 bytes) basis. The data stored in the page buffer 32 is added with an error correction code by the ECC encoder/decoder 34. The page buffer 32 supplies one page data having the error correction code, via the flash I/F sequencer 33 to the flash memories 22a and 22b. Thus, a predetermined data from the electronic apparatus is written in the flash memories 22a and 22b.

Moreover, a data read out from the flash memories 22a and 22b is supplied via the flash I/F sequencer 33 to the pager buffer 32.

The pager buffer 32 stores the data from the flash I/F sequencer 33. Here, the ECC encoder/decoder 34 carries out an error correction processing according to the error correction code added to the data stored in the pager buffer 32. This page buffer 32 reads out page after another the data which has been subjected to the error correction processing and supplies the data to the S/P & P/S sequencer 31. The S/P & P/S sequencer 31 converts the data supplied from the page buffer 32, into a serial data to be transmitted to the aforementioned electronic apparatus.

the command generator 35 generates a control command according to the control data from the S/P & P/S sequencer 31. For example, if the command generator 35 is supplied with a read state register instruction for checking the operation state of the card type memory 1, the command generator 35 decides the setting content of the erroneous erase prevention switch 43 and decides whether to carry out a data writing according to the setting content.

Moreover, the command generator 35 generates a busy command indicating a state of data writing into the storage means 22 or data reading from the storage means 22, and transmits the command via the S/P & P/S sequencer 31 to the electronic apparatus. When the data writing or the data reading is complete, the command generator 35 generates a ready command and transmits the command via the S/P & P/S sequencer 31 to the electronic apparatus.

The configuration ROM 36 contains a version information and an information of an initial value of the card type memory 1. Consequently, when a connection is made between an electronic apparatus and the card type memory 1, the command generator 35 firstly reads out the aforementioned version information and the like from the configuration ROM 36 via the S/P & P/S sequencer 31 and generates a predetermined command according to the information, so as to carry out a predetermined initialization of the card type memory 1.

It should be note that in the aforementioned exam-

ple, explanation has been given on the interface controller A21. The interface controller B24 has an almost identical configuration as the aforementioned interface controller A21 except for the configuration of the command generator.

That is, in the card type memory 1, the aforementioned operation is carried out by selectively connecting the electronic apparatus to the interface controller A21 and the interface controller B24.

Moreover, in the aforementioned example, explanation has been given for a case of a serial interface but the external storage apparatus according to the present invention can also be applied to a parallel interface.

Furthermore, in the aforementioned example, the flash memories are used as a memory, but in the external storage apparatus according to the present invention, it is possible to use a RAM (random access memory) capable of reading out and writing in as well as a ROM other than flash memory.

in the card type memory of the aforementioned example, the storage means is connected to two interface controllers, each having an interface control block of different type, and one of the two interface controllers is selected to an electronic apparatus by connection means. Consequently, it is possible to connect without an adapter to an electronic apparatus having an interface which corresponds to one of the two interface controllers built in this card type memory.

That is, for example, it is possible to write a data from an electronic apparatus such as a still image pickup apparatus, acoustic apparatus, video apparatus or the like to the card type memory of the aforementioned example and connect the card type memory to a computer for example so that the data is read into the computer, all these without using a conversion adapter.

Furthermore, explanation has given on an example of the card type memory having two types of interface control blocks. The external storage apparatus according to the present invention can also have three or more types of interface control blocks. In such a case, a data movement and the like is further facilitated between more electronic apparatuses.

Thus, the external storage apparatus enables to be connected to a plurality of electronic apparatuses having different types of built-in interfaces without using an adapter. As the conversion processing carried out by the interface between an electronic apparatus and the storage means in the external storage apparatus is identical to a conversion when these are directly connected, a high-speed access is enabled regardless of the type of the interface control block in the external storage apparatus.

In summary, embodiments of the invention can provide an external storage apparatus having a plurality of types of built-in interface control blocks enabling a high-speed access regardless of the type of the interface control block.

Claims

1. An external storage apparatus for storing a data from an electronic apparatus, comprising:
 - storage means;
 - interface control blocks of a plurality of types for carrying out a data writing and/or reading into/from said storage means ; and
 - connection means for selecting and connecting one of said plurality of interface control blocks to said electronic apparatus.
2. An external storage apparatus as claimed in Claim 1, wherein said connection means is constructed so as to select one of said plurality types of interface control blocks according to a control from said electronic apparatus.
3. An external storage apparatus as claimed in Claim 1, wherein one of said interface control blocks of plurality of types is an interface control block for USB (Universal Serial Bus).
4. An external storage apparatus as claimed in Claim 1, wherein one of said interface control blocks of plurality of types is an interface control block for the IEEE 1394.
5. An external storage apparatus as claimed in Claim 1, wherein said interface control blocks of plurality of types are for use in a serial interface.
6. An external storage apparatus as claimed in Claim 1, wherein said interface control blocks of plurality of types are for use in a parallel interface.
7. An external storage apparatus as claimed in Claim 1, wherein said storage means is realized by using a flash memory.
8. A memory system comprising an electronic apparatus and an external storage apparatus connected to said electronic apparatus for storing a data from said electronic apparatus, wherein said external storage apparatus includes:
 - storage means;
 - interface control blocks of a plurality of types for carrying out a data writing and/or reading into/from said storage means; and
 - connection means for selecting and connecting one of said interface control blocks of plurality of types to said electronic apparatus.
9. A memory system as claimed in Claim 8, wherein said electronic apparatus transmits a signal for selecting one of said interface control blocks of plurality of types, to said external storage apparatus; and said connection means, according to said signal, selects one of said interface control blocks of plurality of types
10. A memory system as claimed in Claim 8, wherein one of said interface control blocks of plurality of types is an interface control block for USB (Universal Serial Bus).
11. A memory system as claimed in Claim 8, wherein one of said interface control blocks of plurality of types is an interface control block for the IEEE 1394.
12. A memory system as claimed in Claim 8, wherein said interface control blocks of plurality of types are for use in a serial interface.
13. A memory system as claimed in Claim 8, wherein said interface control blocks of plurality of types are for use in a parallel interface.
14. A memory system as claimed in Claim 8, wherein said storage means is realized by using a flash memory.

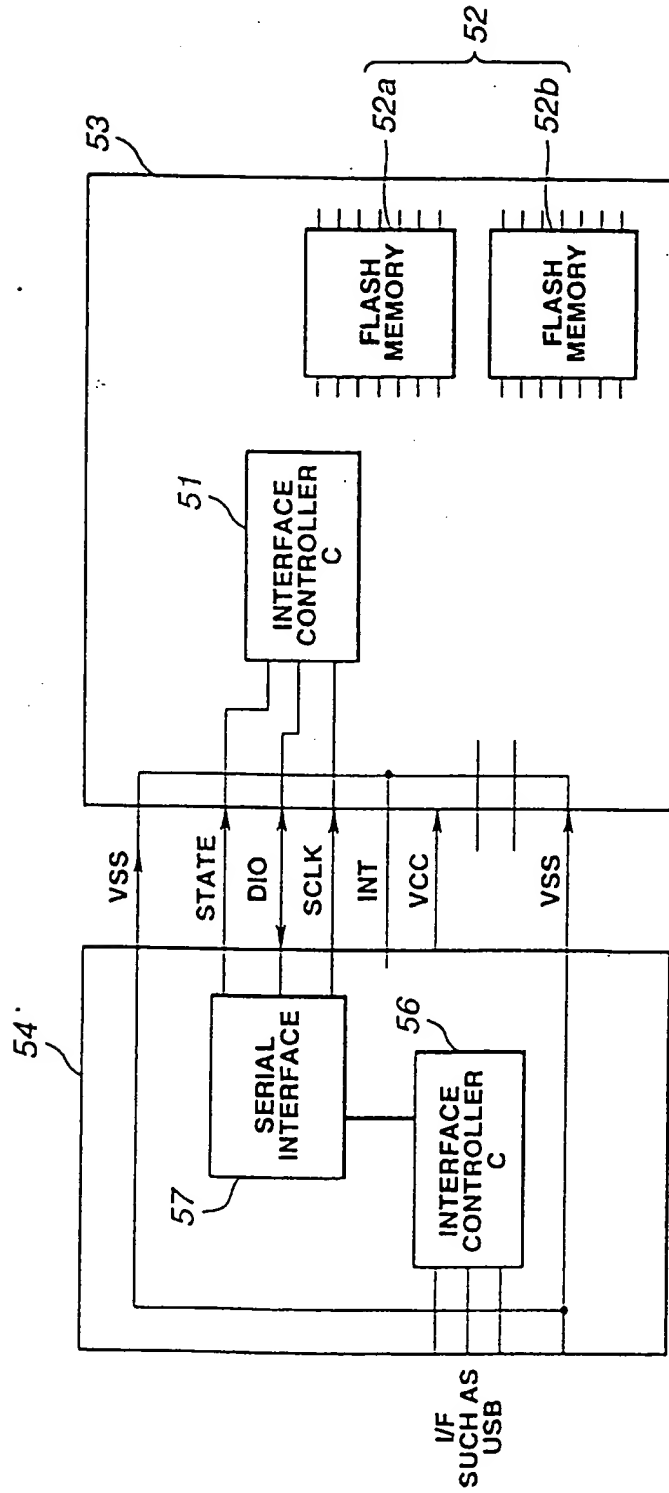


FIG.1

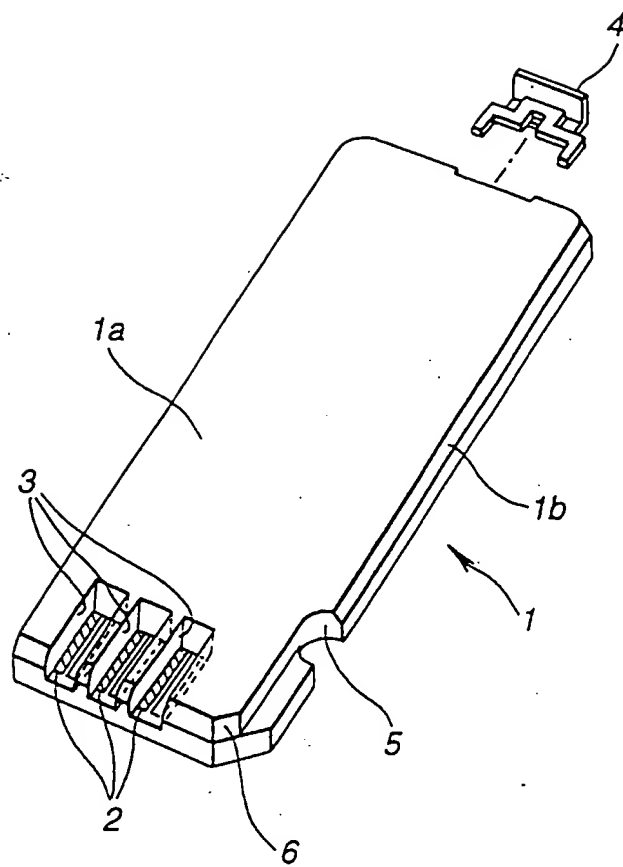


FIG.2

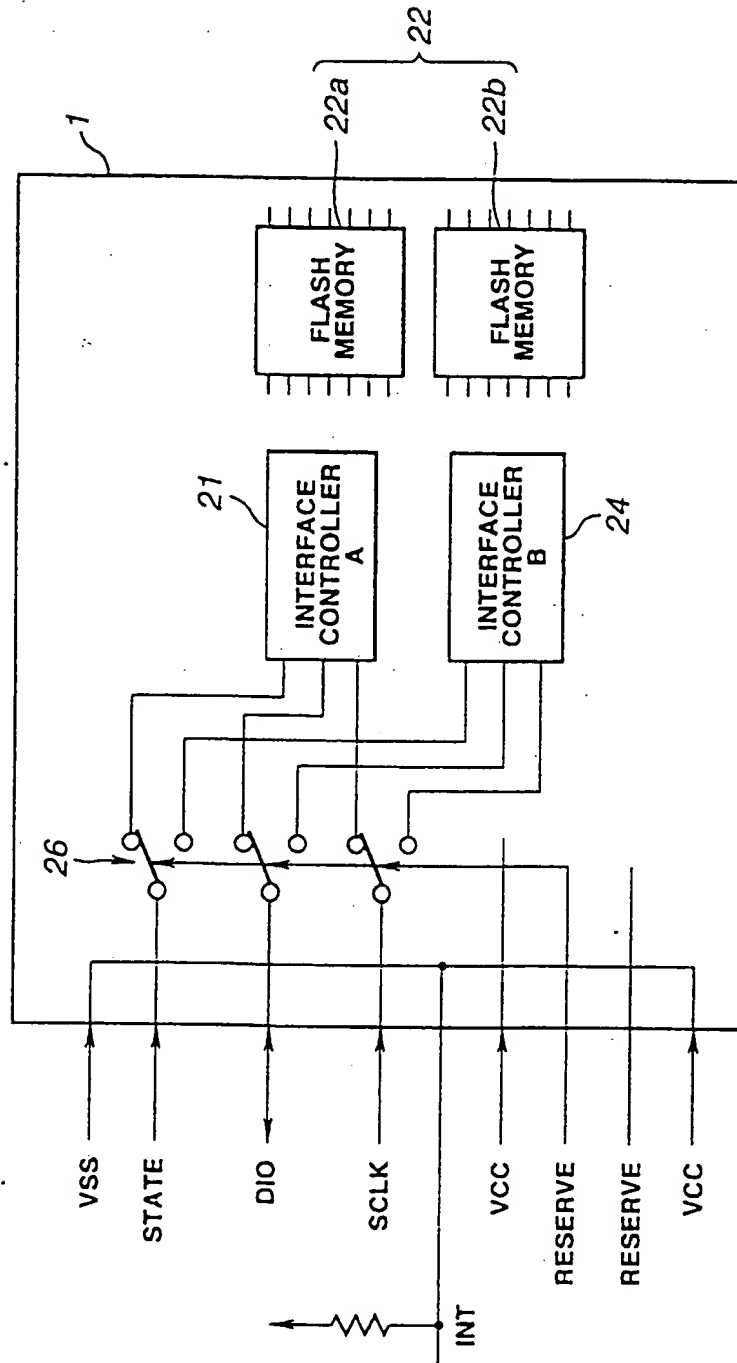


FIG.3

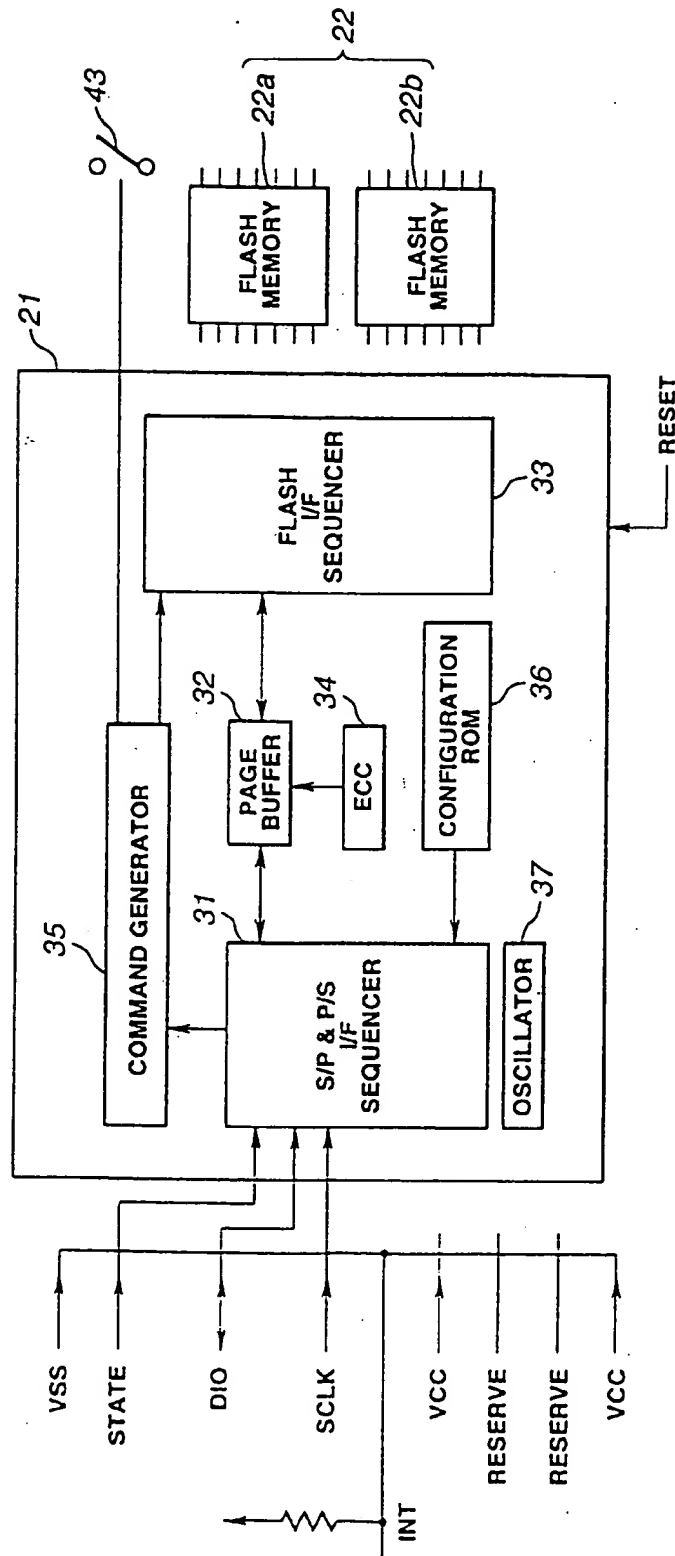


FIG.4

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Application Number
EP 98 30 4354

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	US 5 420 412 A (KOWALSKI JACEK) 30 May 1995 * column 2, line 43 - line 66 * * column 4, line 11 - line 68 * * column 5, line 11 - column 6, line 58 * * abstract; claims 1.2; figure 1 * ---	1,2,5-9, 12,13 3,4, 10-14	G06K19/07 G06F13/38
X A	US 5 581 708 A (IIJIMA YASUO) 3 December 1996 * column 1, line 21 - column 2, line 2 * * column 2, line 24 - column 3, line 58 * * abstract; claims 1.2; figure 1 * ---	1,8 2-7,9-14	
A	EP 0 513 507 A (TOKYO SHIBAURA ELECTRIC CO) 19 November 1992 * abstract * -----	1-14	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06K G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 28 September 1998	Examiner Nguyen Xuan Hiep, C
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